Design and Testing of 400G/800G Optical and Electrical Network

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2021.12

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Optical Network

OPTICAL

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Standards update

I will focus on new specifications and measurements

- Standards recently completed
 - IEEE 802.3 cu: 100 Gb/s per lane
 - IEEE 802.3 cn: 50 Gb/s, 200 Gb/s, and 400 Gb/s over greater than 10 km
 - Open Eye MSA 50 Gb/s
- Standards in development
 - IEEE 802.3 db: 100 Gb/s per lane on multimode fiber
 - IEEE 802.3 cw: Coherent systems for data center interconnect
 - 800G MSA: includes 200 Gb/s per lane using
- Standards on the horizon
 - IEEE B400G: "What is next to go to 800Gb/s and 1.6 Tb/s systems"



TDECQ references

- <u>https://www.keysight.com/us/e</u> n/assets/7018-06485/whitepapers/5992-3635.pdf
- <u>https://www.keysight.com/us/e</u> n/assets/7018-06506/whitepapers/5992-3676.pdf
- TDECQ test time has been reduced from about 5 seconds to 3 seconds with latest firmware (6.8)



TDECQ Part 1 Making Accurate and Repeatab

TDECQ Overview

TDECQ is the acronym used to describe quaternary". This is a power penalty met is required from a transmitter, relative to both non-ideal transmitter waveforms ar is similar to the transmitter dispersion p

TDECQ Part II Manufacturing Test Recommendations

TDECQ Overview

TDECQ (Transmitter Dispersion and Eye Closure Quaternary) is the primary metric defining the performance of an optical transmitter used in a PAM4-based Ethernet link. It is found in IEEE 802.3bs (400 Gb/s optical), IEEE 802.3cd (50 and 100 Gb/s optical), Fiber Channel PI-7 (64GFC), and is being leveraged into other PAM4-based optical standards. TDECQ is intended to be the equivalent of transmitter dispersion penalty (TDP) metrics developed in earlier NRZ-based Ethernet standards. TDP has generally not been implemented in manufacturing test processes due to test time and complexity. Instead, results have been correlated to the simpler mask margin and hit ratio tests.

While the industry has decades of experience to draw upon for eye mask testing, much of that experience does not directly translate to TDECQ measurements.

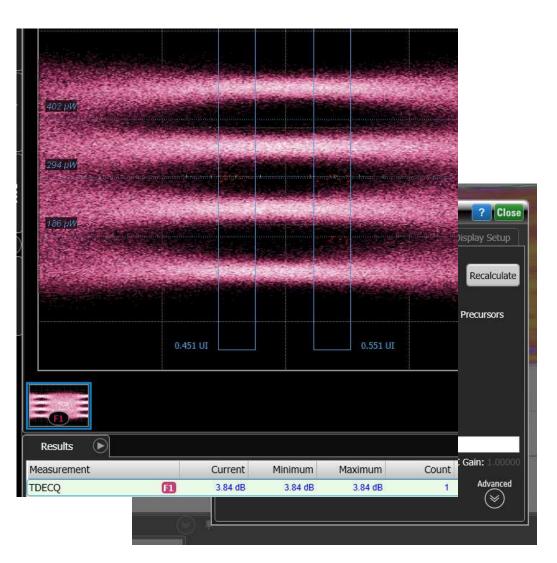
WHITE PAPER

Two factors have led the adoption of TDECQ in manufacturing test for PAM4 transmitters instead of the continued use of eye mask testing. First, the transmitter test requires the use of an EEE (Each Ecouverd Ecuvation to ensure the output Second



TDECQ is used on all PAM4 TX standards

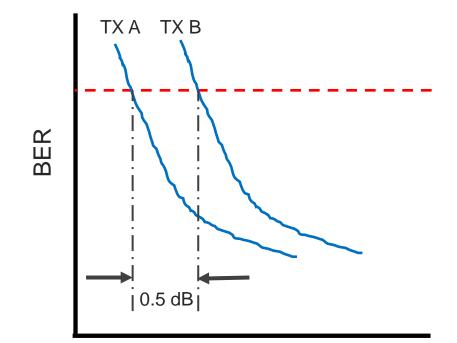
- Transmitter Dispersion and Eye Closure
 Quaternary
- The transmitter under test is passed through a virtual equalizer that emulates the equalization that the real system receiver will perform
- Compares the equalized eye openings against a virtual ideal reference transmitter (a signal with the same OMA but with ideal linearity and no eye closure)





A practical view of TDECQ

- Definition: How much extra power is required from the transmitter, relative to an ideal transmitter, to compensate for the eye closure
- TDECQ should predict relative shifts in receiver sensitivity at the system level due to TX eye quality
- If transmitter A has a TDECQ of 2.7 dB and transmitter B has a TDECQ of 3.2 dB, <u>when these are connected</u> to a real receiver, sensitivity curves should be separated by 0.5 dB (3.2 – 2.7) at uncorrected SER limit



Key Point: This works well when the virtual receiver used for TDECQ analysis correctly emulates the physical receiver used in the sensitivity measurements Receiver input power

IEEE 802.3 cn

50/200/400 GB/S OVER GREATER THAN 10 KM

- Although this focuses on a long reach system, it also impacted the clauses for shorter reaches including 50, 200 and 400 Gb/s at shorter spans (e.g. 200/400Gbase-DR4, 200/400Gbase-FR4, 200/400Gbase-LR4 etc.)
- The TDECQ reference receiver definitions for 802.3 bs and 802.3 cd are slightly different
 - 802.3 cd uses a higher capability receiver with the ability to optimize the decision thresholds
 - A signal with some nonlinearity in the PAM4 levels will have a lower TDECQ penalty when measured with the 802.3cd settings compared to the 802.3 bs settings
- The 802.3cn project updated the TDECQ definitions so that the .bs clauses are now the same as the .cd clauses
- When making 802.3bs measurements, use the 802.3 cd setups!



802.3 cu

100 AND 400 GB/S OVER SMF AT 100 GB/S PER WAVELENGTH

- TDECQ measurements were leveraged from 802.3cd. No changes to the measurement
- A huge debate raged in this committee:
- What is 10 log Ceq, what does it mean, and how should we use it?
- This term was introduced in the 802.3cd project and was not well understood

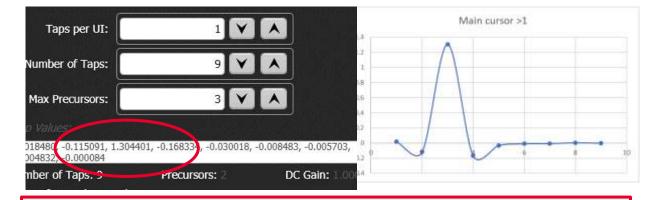
| Description | Value | Unit | |
|---|--------------------|------------|--|
| Signaling rate (range) | $53.125\pm100~ppm$ | GBd | |
| Modulation format | PAM4 | | |
| Wavelength (range) | 1304.5 to 1317.5 | nm | |
| Side-mode suppression ratio (SMSR), (min) | 30 | dB | |
| Average launch power (max) | 4 | dBm | |
| Average launch power ^a (min) | -2.9 | dBm | |
| Outer Optical Modulation Amplitude (OMA _{outer}) (max) | 4.2 | dBm | |
| Outer Optical Modulation Amplitude (OMA _{outer}) (min) ^b | -0.8 | dBm | |
| Launch power in OMA _{outer} minus TDECQ (min): for extinction ratio ≥ 5 dB for extinction ratio < 5 dB | -2.2 -1.9 | dBm dBm | |
| Transmitter and dispersion eye closure for PAM4 (TDECQ) (max) | 3.4 | dB | |
| $\text{TDECQ} - 10\log_{10}(C_{\text{eq}})^{\text{c}} \text{ (max)}$ | 3.4 | dB | |
| Average launch power of OFF transmitter (max) | -15 | dBm | |
| Extinction ratio (min) | 3.5 | dB | |
| Transmitter transition time (max) | 17 | ps | |

Table 140-6—100GBASE-DR transmit characteristics

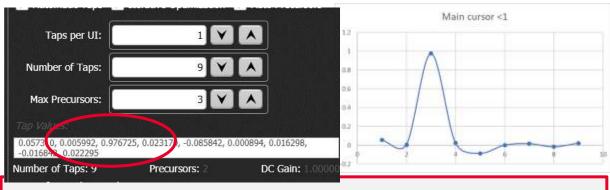


Ceq is derived from the virtual equalizer tap values

- For normalized taps (sum of tap weights =1), if the main cursor is greater than 1, the equalizer is correcting for a low-pass system.
 - The larger the difference between the main cursor and its neighboring pre or post cursors the more the equalizer is attempting to boost high frequencies.
 - This would be a more typical case, where the equalizer is required to open the eye
 - Boosting high frequencies results in system noise gain.
 Ceq is >1 or > 0 dB
- Some intuition into the equalizer response can be gained from plotting the tap weights and viewing the relative impulse response (narrow for high-pass, wide for low-pass)
- A low pass system will reduce noise. Ceq <1 or < 0 dB



EQ impulse response is 'narrow' and will boost high frequencies (Ceq >1)



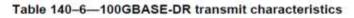
EQ impulse response is wider, high frequencies attenuated and Ceq <1



What is the "TDECQ – 10log Ceq"

- You are penalized if Ceq is less than 1
- This is the case where the equalizer is trying to reduce the system bandwidth
- What is being prevented??
- Possible example: A very fast, overequalized transmitter that could be very difficult for a receiver to work with

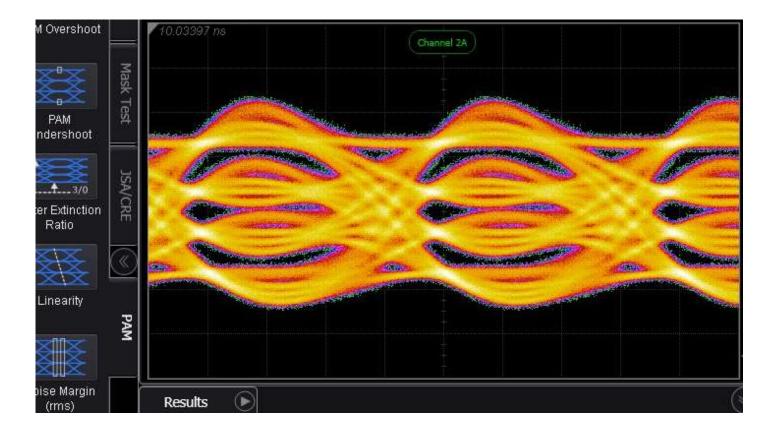
| Description | Value | Unit | |
|---|--------------------|------------|--|
| Signaling rate (range) | $53.125\pm100~ppm$ | GBd | |
| Modulation format | PAM4 | - 1 | |
| Wavelength (range) | 1304.5 to 1317.5 | nm | |
| Side-mode suppression ratio (SMSR), (min) | 30 | dB | |
| Average launch power (max) | 4 | dBm | |
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| Launch power in OMA _{outer} minus TDECQ (min): for extinction ratio ≥ 5 dB for extinction ratio < 5 dB | -2.2 -1.9 | dBm dBm | |
| Transmitter and dispersion eye closure for PAM4 (TDECQ) (max) | 3.4 | dB | |
| $TDECQ = 10\log_{10}(C_{eq})^{c} (max)$ | 3.4 | dB | |
| Average taunch power of OFF transmitter (max) | -15 | dBm | |
| Extinction ratio (min) | 3.5 | dB | |
| Transmitter transition time (max) | 17 | ps | |





A case study

- Could this signal pass the TDECQ test??
- Would the TDECQ 10 log Ceq parameter tell us anything?

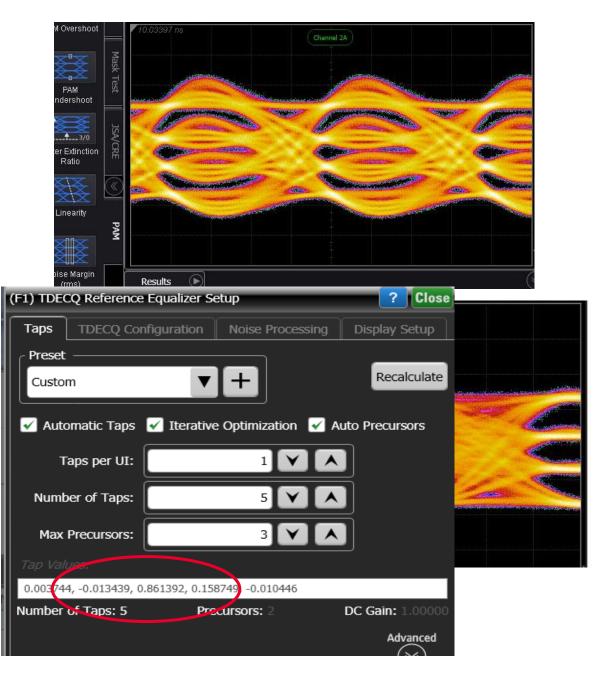




Some surprising results

- The TDECQ penalty was negative! (lower power penalty than what an ideal signal without equalization can achieve)
- How does this work and what clues can we look for?
- Main cursor is <1
- Ceq is -0.7 dB

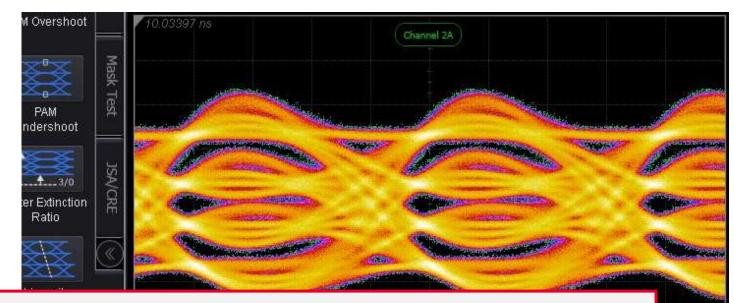
The TX eye is opened by reducing high frequencies that caused severe overshoot. The equalizer impulse response is wider, resulting in Ceq <1





TDECQ cannot protect real receivers from some eye impairments

- TDECQ provides insight into link budgets and system level receiver sensitivity. It provides almost no information on signal impairments that might overload the front end of a receiver such as high overshoot (other than what the Ceq parameter implied)
- An eye mask test for NRZ limited overshoot and undershoot that might overdrive a receiver. But there is no PAM4 eye mask in 802.3 standard



The TDECQ for this signal was ~0 dB, and Ceq -0.7 dB. The TDECQ – 10 log Ceq metric was + 0.7 dB, well within specs. This approach was not effective in screening out this type of signal



802.3cu developed tests to directly limit overshoot and undershoot

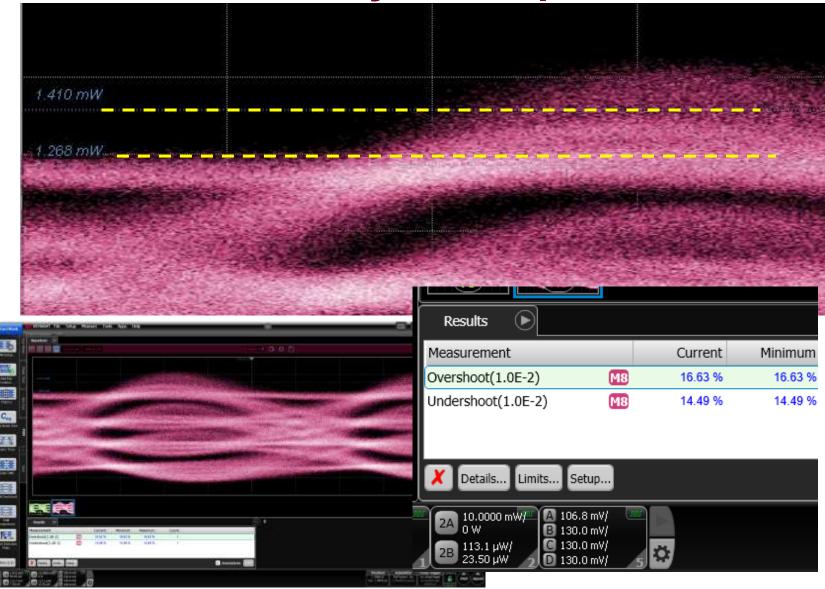
- Keysight developed an overshoot/undershoot test method and presented it to the 802.3cu project
- A transceiver vendor used the test method and measured a large sample size of transmitters
- Conclusions:
 - TDECQ works very well to predict the impact eye closure will have on system receiver sensitivity, but it cannot predict how waveform problems might impact the front end of a receiver
 - Some overshoot can be good, but too much can lead to error floors
 - Using the Keysight method, a 22% limit is good at screening out problematic transmitters without placing a large burden on most transmitter. This was written into the standard

Expect that some type of overshoot test will be required for all new PAM4 standards



Overshoot measurement for closed eye example

- One level measured at 1.288 mW
- Overshoot threshold for a 1e-2 setting at 1.41 mW (the level for which no more that 1 in every 100 samples (1e-2) reside above)
- The current spec limit is 22%, so this signal is not rejected. The overshoot must be severe to fail the test



IEEE 802.3 db

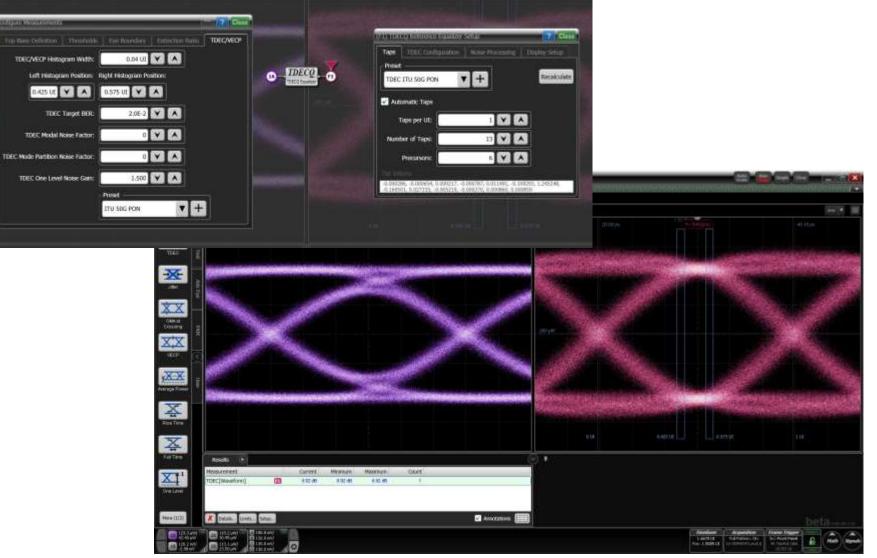
100/200/400 GB/S SHORT REACH FIBER

- Will use 50 Gbaud transmitters
- Will use TDECQ as the primary transmitter test metric
- Assumes that system receivers will have more capabilities than the receivers used in earlier standards that use TDECQ
- Using multimode fiber, so the primary dispersion mechanism is modal rather than chromatic
 - Modal dispersion can be emulated with a low-pass filter rather than requiring real fiber for single-mode transmitters



Key changes for TDECQ analysis

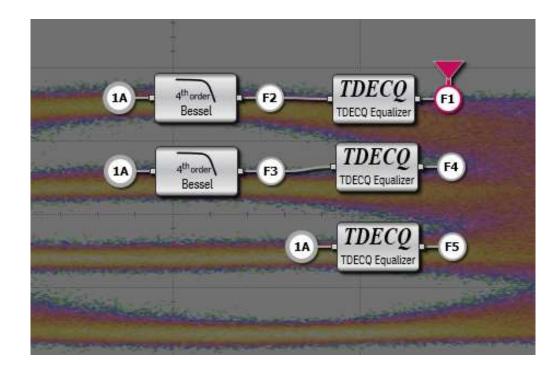
- Reference equalizer will have 9 taps rather than 5
- Reference receiver decision thresholds allowed to optimize for lowest TDECQ penalty within a 2% of OMA limit (rather than 1%)





Emulating model dispersion

- Earlier multimode standard aggregated the low pass response of the fiber and the reference receiver bandwidth into one observation bandwidth that defined the DCA channel bandwidth
- 802.3 db has split apart the fiber model from the reference receiver into separate functions
- With a single waveform acquisition using a 26.6 GHz DCA channel BW, TDECQ can be measured for different fiber spans by creating different low-pass blocks to pass the signal through
 - TECQ can be obtained from the same signal by observing it prior to the fiber emulation
 - Very fast, very flexible, no new DCA hardware configurations





50G ITU PON (ITU G.9804.3)

- Will have the NRZ eye mask test
- Developed a new TDEC (before there was TDECQ for PAM4, TDEC was developed for NRZ)
- Keysight is worked directly with participants to define the reference receiver bandwidths and measurement methods



A look into the future

- The next project in IEEE is "Beyond 400G (B400G)"
- 5-year timeline
- Very early in the process with only very basic definitions being discussed
- 800G MSA: Early specifications with definitions for 200 Gb/s lanes using 100 Gbaud transmission
- Will use TDECQ, considering a 21-tap virtual equalizer



Electrical Network

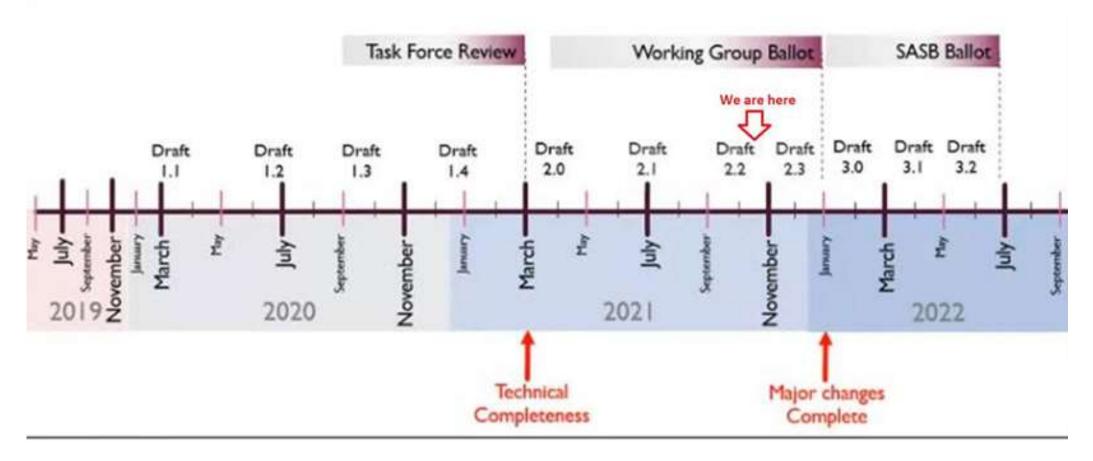
ELECTRICAL

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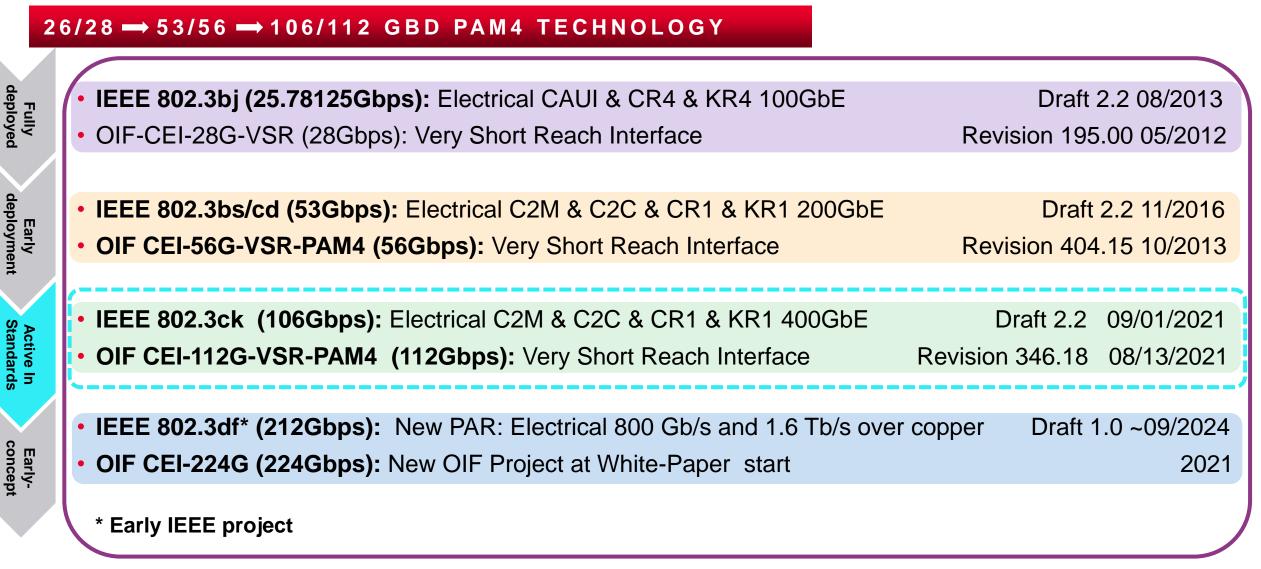


IEEE 802.3ck Schedule (as of 10/04/2021)

IEEE P802.3 P802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces (100GEL) Task Force Adopted timeline



"Active" High Speed Networking Electrical Standards





Emerging 100G Electro/Optic Specifications

26/28 → 53/56 → 106/112 GBD PAM4 TECHNOLOGY

- IEEE 802.3ck (106Gbps): Electrical C2M & C2C & CR1 & KR1 400GbE
- IEEE 802.3cu (106Gbps): 10Km, Single-Mode Optical Fiber at 106 Gbps per λ
- IEEE 802.3db (106Gbps): 50M, Multimode Optical Fiber at 106Gbps per Fiber
- IEEE 802.3ct (106Gbps): 80Km, DWDM (dense wavelength division multiplexing)

Draft 2.2 09/01/2021 Published Feb 2021 Draft 1.2 July 2021 Published July 2021

Project Start 355.00 11/02/2020

- OIF CEI-112G-MCM (112Gbps): 3D stacked Chip to Chip (CNRZ-5)
 OIF CEI-112G-XSR (112Gbps): Chip to Chip, Chip to Co-Pkg Optics
 OIF CEI-112G-XSR+ (112Gbps): Chip to Chip, Chip to Near Pkg Optics
 OIF CEI-112G-VSR (112Gbps): Chip to Module
 OIF CEI-112G-MR (112Gbps): Chip-to-Chip & Midplane Applications
 OIF CEI-112G-LR (112Gbps): Backplane or Passive Copper Cable
 Revision 171.08 07/31/2019
 Revision 065.10 08/31/2021
 Project Start 431.03 08/06/2021
 Revision 346.18 08/13/2021
 Revision 340.07 08/06/2021
 Revision 212.14 08/06/2021
- OIF CEI-CPO (112Gbps) : Co-Pkg Optics

Active In Standards



"Active" '800G Class' Standards

53/56 GBD PAM4, 106/112G LANE RATES ("112G")

 IEEE 802.3ck (106Gbps): Electrical C2M & C2C & CR1 & KR1 400GbE & 800G 802.3cu (106Gbps): 10Km, Single-Mode Optical Fiber at 106 Gbps per λ 802.3db (106Gbps): 50M, Multimode Optical Fiber at 106Gbps per Fiber 802.3ct (106Gbps): 80Km, DWDM (dense wavelength division multiplexing)

• OIF CEI-112G

- 5 reaches PAM4, CNRZ-5
- MCM: Multi-Chip Module, 348.0 Gbps over six wires using Chord Signaling (CNRZ5)
- XSR Die to Die: 36 to 58 Gsym/s with up to 10 dB loss, bump to bump, at the Nyquist frequency, with no connector, for system in package (SIP) applications.
- XSR+ Die to Die: 36-54Gsym/s Project Start, basically XSR but with a connector.
- VSR C2M: 36.0 to 58.0 Gsym/s with up to 12 dB loss at the Nyquist frequency, including one connector.
- MR C2C: 36 to 58 Gsym/s with up to 20 dB loss at the Nyquist frequency, including one connector.
- LR C2C: 36 to 58 Gsym/s with up to 28 dB loss at the Nyquist frequency, including two connectors.
- Fibre Channel PI-8 128GFC
- IBTA NDR (53.125GBaud)

Draft 2.1 July 2021 Published Feb 2021 Draft 1.2 July 2021 Published July 2021

Leveraging IEEE 802.3ck

Leveraging IEEE 802.3ck

| | | | IEEE Standard | Symbol Rate | Format |
|--------------------------|----------------------|--|---|-------------|--------------|
| | | Standards OverviewECT LANDSCAPE"802.3bs/cd | 200GAUI-4 C2C 400GAUI-8 C2C 50GAUI-1 C2C 100GAUI-2 C2C | 26.5625 Gbd | PAM4 |
| | 5 | chip to chip LR across backplane; max 2 connectors Switch card | 200GAUI-4 C2M 400GAUI-8 C2M 50GAUI-1 C2M 100GAUI-2 C2M | 26.5625 Gbd | PAM4 |
| | - | chip to chip (max 1 connector) | 50GBASE-KR 100GBASE-KR2 200GBASE-KR4 | 26.5625 Gbd | PAM4 |
| | e to die U n MCM) | SR chip to optical engine (inside module) | 50GBASE-CR 100GBASE-CR2 200GBASE-CR4 | 26.5625 Gbd | PAM4 |
| | | chip to plugable optical module | 400GBASE-DR4 | 53.125 Gbd | PAM4 (SM) |
| | 10 | VSR EEEE | 100GAUI-1 C2M 200GAUI-2 C2M 400GAUI-4 C2M | 53.125 Gbd | PAM4 |
| OIF-CEI | IEEE | 802.3ck | 100GAUI-1 C2C 200GAUI-2 C2C 400GAUI-4 C2C | 53.125 Gbd | PAM4 |
| VSR | C2M | 0.7 | 100GBASE-KR 200GBASE-KR2 | 53.125 Gbd | PAM4 |
| MCM/XSR | C2C | | 400GBASE-KR4 100GBASE-CR | 53.125 Gbd | PAM4 |
| LR | KR/CR | - | 200GBASE-CR 200GBASE-CR2 400GBASE-CR4 | 53.125 GDd | r'Alvi4 |
| KEYSIGHT TECHNOLOGIES | - | Keysight High-Speed Digital Test Forum 是德科技高速數位量測論壇 | | | 26 |

-

100G (53.125GBd or 56GBd) interface electrical conformance

802.3CK AND OIF-CEI-VSR-112G-PAM4 PHY VALIDATION

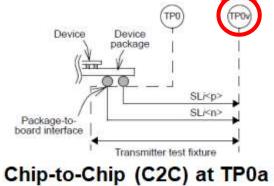


Keysight High-Speed Digital Test Forum 是德科技高速數位量測論壇

100G Transmitter Test Points

IEEE 802.3CK ELECTRICAL TX TEST POINTS (C2C, C2M)



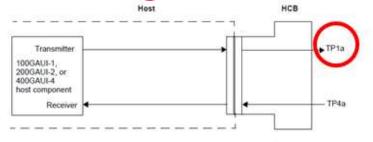


(custom fixture)

•Measured without Ref RX Equalizer

Jitter, SNDR, rise time...

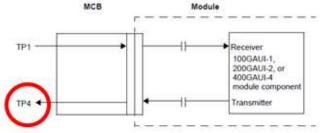




Chip-To-Module (C2M) at TP1a (use compliant fixture)

•Measured with Ref RX Equalizer

Vec, EH



Chip-to-Module Module Output (C2M) at TP4 (use compliant fixture)

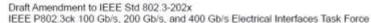
•Measured with Ref RX Equalizer





Test Fixture loss

SPECS ARE DEFINED DOWNSTREAM OF THE MATED TEST FIXTURE



IEEE Draft P802.3ck/D2.2 1st September 2021

$$ILdd_{MIFref}(f) = 0.942(0.471\sqrt{f} + 0.1194f + 0.002f^2)$$

(162B-5)

for 0.01 GHz $\leq f \leq$ 50 GHz

where

 ILdd_MTFref(f)
 is the reference differential-mode to differential-mode insertion loss of the mated test fixture differential-mode to differential-mode insertion loss in dB at frequency f

 f
 is the frequency in GHz

The mated test fixtures differential-mode to differential-mode insertion loss limits are illustrated in Figure 162B-3.

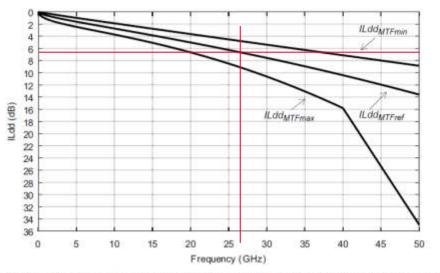


Figure 162B-3-Mated test fixtures differential-mode to differential-mode insertion loss

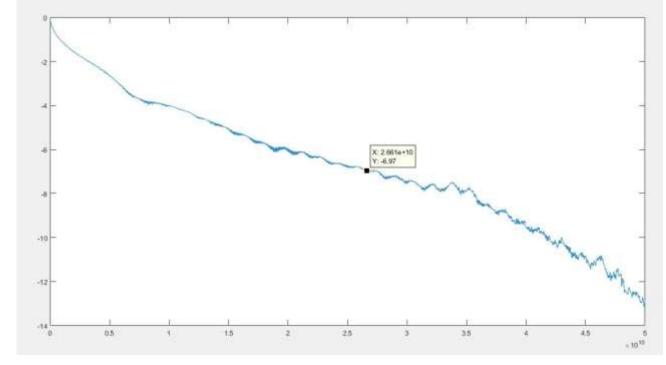


Figure 162B-3 illustrates allowable test fixture SDD21 tolerances

Top SDD21 illustrates an example of a conformant test fixture

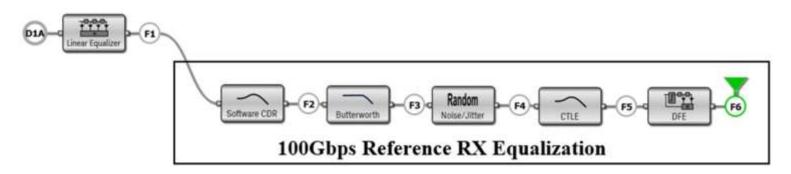


Tx and Rx Reference Equalization

TX + RX EQUALIZATION NEEDS TO BE INTEGRAL TO VEC EVALUATION

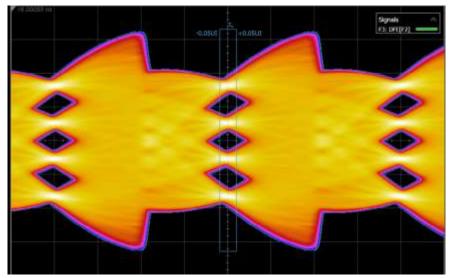
- The mainstream move to higher order direct modulation methods such as in PAM4, has resulted in several key architectural shifts: Signal processing is required with increasing complexity
- Native error rates in the 10E-4 error ratio arena are now main stream, with heavy reliance on Forward Error Correction (FEC) to reduce error rates to below ~10E-13. FEC operates on the premise that the high intrinsic error rate emanates from random errors with a Poisson distribution
 - Deviation from this distribution (e.g. error bursts) significantly impacts system margin
- System level transmitter and reference receiver equalization to establish an operational low error rate link
 100Gbps TX Equalization

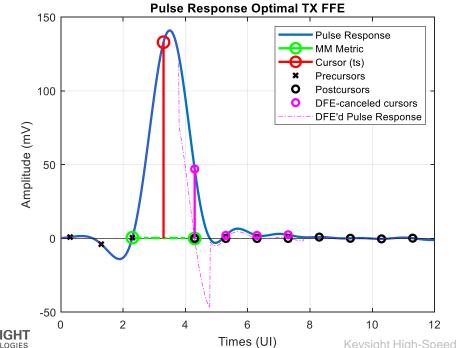
(e.g. Feedforward Equalizer)





TX FFE + RX CTLE + RX DFE : Compound Equalization

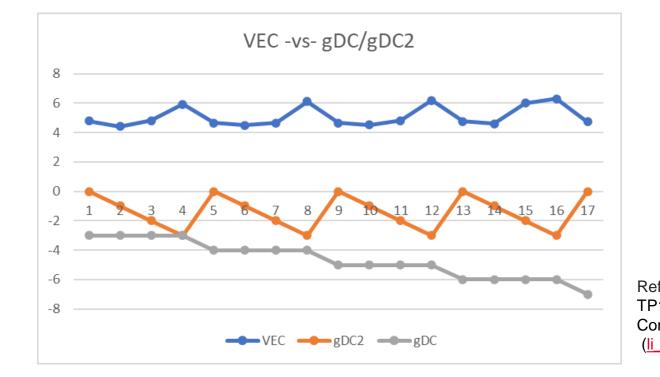


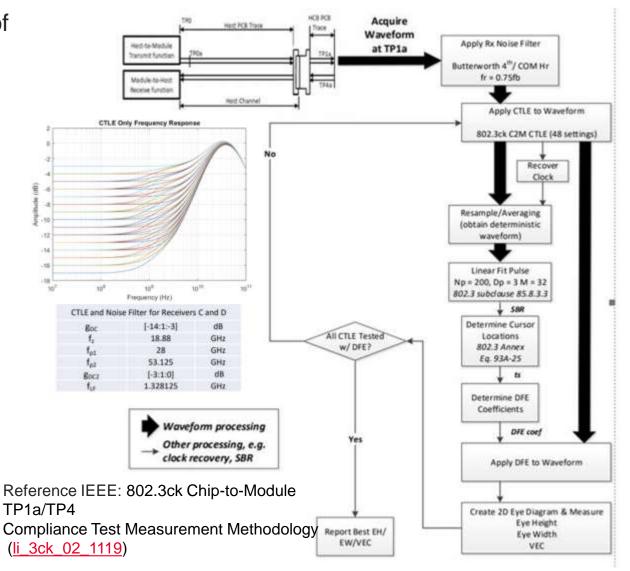


- Current 100G standards call out the use of a Mueller-Muller digital synchronization method of clock recovery
 - This technique extracts a leading phase of the main cursor in a way to offer the DFE a higher effective operating gain and greatly improves the cursor cancelation capability
- The optimal equalizer filter coefficients are determined through a grid search for the TX FFE first precursor, first post cursor, and CTLE/DFE settings that yield the best VEC with sufficient Eye Height
- DFE tap limits are restricted and care needs to be exercised not to exceed these

TX FFE + RX CTLE + RX DFE : Composite effects

- This is a flow diagram which illustrates the mechanics of how a 100G filter optimization grid search would cycle through the equalizer solution space to determine empirically the optimal VEC
- It's quickly apparent that the non-linear behavior of the DFE presents a complex solution landscape







P802.3ck Eta_0

NOISE REQUIREMENTS ASSOCIATED WITH ETA_0

Draft Amendment to IEEE Std 802.3-202x IEEE P802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force IEEE Draft P802.3ck/D2.2 1st September 2021

120G.5.2 Eye opening measurement method

The eye opening parameters eye height and VEC are measured with the effect of a reference receiver which includes receiver input referred noise, a continuous-time filter as defined in 93A.1.4.3, a receiver noise filter as defined in 93A.1.4.1, and a decision-feedback equalizer as defined in 93A.1.6, using the parameters specified in Table 120G–11. All parameters in Table 120G–11 apply to TP1a, TP4 far-end, and TP4 near-end unless indicated otherwise. The pattern used for output eye diagram measurements is PRBS13Q. Unless specified otherwise the probabilities are relative to the number of PAM4 symbols measured. Eye height and VEC parameters are defined by the following procedure.

| One-sided noise spectral density | η ₀ | $4.1\times10^{\text{-8}}$ | V ² /GHz |
|----------------------------------|----------------|---------------------------|---------------------|



Intrinsic Noise Profile of Oscilloscopes

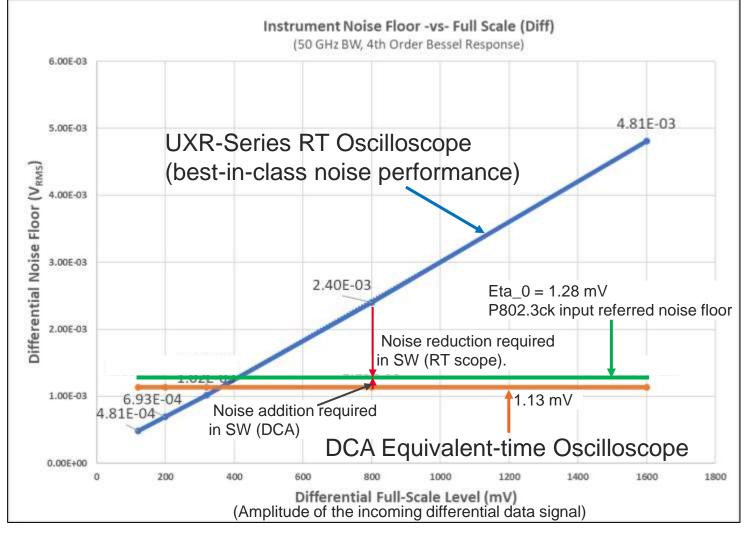
IMPORTANT PARAMETER FOR COMPLIANT "RX INPUT REFERRED NOISE" RESULTS

Real-time Oscilloscope

- Intrinsic noise depends on channel gain and offset setting
- SNR is constant noise scales with signal amplitude.
- Scope noise depends on the amplitude of the input signal

Equivalent-time Oscilloscope

- Noise is constant and independent of channel gain
- SNR improves with higher amplitude signals.
- Scope noise is independent of input signal amplitude

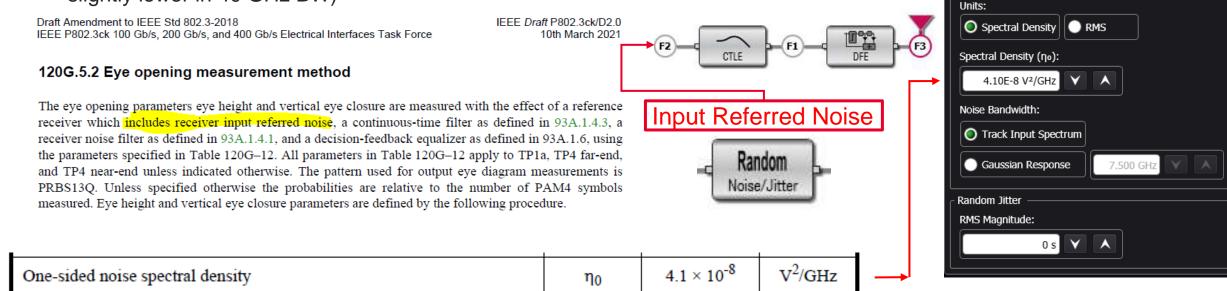


Input Referred Noise on Sampling (need to add noise)

FLEXDCA REV 6.60 ADDS SUPPORT FOR IEEE802.3CK FLOOR ETA_0

IEEE 802.3ck adds "Input Referred Noise":

- Add a fixed (and known) amount of receiver noise at the input to the CTLE
- Eta_0 = 1.28 mV rms Differential (in a 40 GHz BW) Table 120G-9 defines eta_0 in V²/GHz
- FlexDCA uses intrinsic noise measured during module cal and automatically RSS add noise to meet requirement (N1060A Diff Noise = 1.1 mV rms in 50 GHz BW, slightly lower in 40 GHz BW)



? Close

F2) Random Noise/Jitter Setup

Bandwidth Limited

Display Setup

 $\mathbf{\nabla}$

🔵 White

Operator Setup

IEEE 802.3ck

Random Noise

Spectrum:

Preset

Input Referred Noise on Realtime Instrumentation

Similar Eta_0
 objectives on a
 Realtime
 instrument have
 been recently
 introduced

 12 edge slew-rates are fully characterized, and the AM/FM conversion characteristics accounted for at each level traversal





P802.3ck Electrical/Jitter Specs

100G C2C CHIP TO CHIP PHY REQUIREMENTS

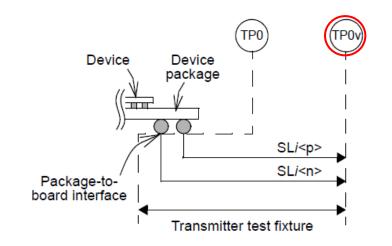


Figure 163–3—Transmitter test fixture and test points



Draft Amendment to IEEE Std 802.3-202x IEEE P802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force IEEE Draft P802.3ck/D2.2 1st September 2021

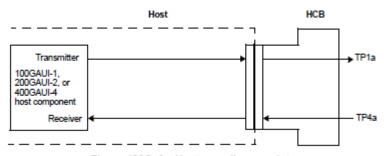


| Parameter | Reference | Value | Units |
|---|--|---|----------------|
| Signaling rate, each lane (range) | | $53.125\pm50~\mathrm{ppm}^{\mathrm{a}}$ | GBd |
| | | | |
| Signal-to-noise-and-distortion ratio, SNDR (min) | 162.9.3.3 | 32.5 | dB |
| Residual intersymbol interference, ISI_RES (max) | 163.9.2.6 | -31 | dB |
| Output jitter J _{RMS} (max) J4u (max) Even-odd jitter (max) | 120F.3.1.3 120F.3.1.3 120F.3.1.3 | 0.023 0.118 0.025 | UI UI UI |

TP0v evaluation is performed with TX FIR only 4th order Bessel Thompson 40GHz



TP1a and TP4



Eye Tests/VEC, use CTLE/DFE, all other tests are measured through 4th order Bessel Thompson (no CTLE/DFE)

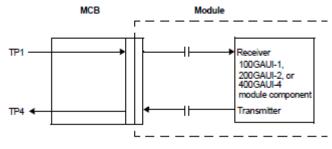


Figure 120G-4-Module compliance points

Table 120G-3-Module output characteristics (at TP4)

| • | | | | - |
|--|------------|---------------------|-------|----------|
| Parameter | Reference | Value | Units | |
| Signaling rate, each lane (nominal) | | 53.125 ^a | GBd | 1 |
| AC common-mode output voltage (max, RMS) | 120G.5.1 | 17.5 | mV | Ī |
| Differential peak-to-peak output voltage (max) | 120G.5.1 | 900 | mV | I |
| Eye height, differential (min) | 120G.3.2.2 | 15 | mV | |
| Vertical eye closure (max) | 120G.3.2.2 | 12 | dB | U |
| Common-mode to differential return loss (min) | 120G.3.1.1 | Equation (120G-1) | dB | Ī. |
| Effective return loss, ERL (min) | 120G.3.2.3 | 8.5 | dB | Ī |
| Differential termination mismatch (max) | 120G.3.1.3 | 10 | % | Ī |
| Transition time (min, 20% to 80%) | 120G.3.1.4 | 8.5 | ps | Ι |
| DC common-mode voltage (min) ^b | 120G.5.1 | -350 | mV | I |
| DC common-mode voltage (max) ^a | 120G.5.1 | 2850 | mV | Ι |
| | | | | |

^aThe signaling rate range is derived from the PMD receiver input. ^bDC common-mode voltage is generated by the host. Specification includes effects of ground offset voltage.

Table 120G-5-PCB length for module output measurements

| Module output mode | Host channel type | PCB length, zp (mm) |
|--------------------|-------------------|---------------------|
| Short | near-end | 0 |
| Short | far-end | 160 |
| Long | near-end | 80 |
| Long | far-end | 244.7 |

Jse CTLE/DFE

Figure 120G-3-Host compliance points

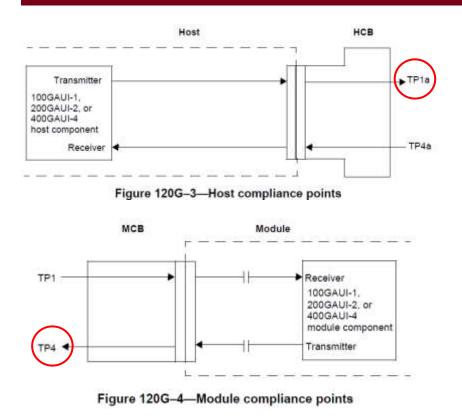
Table 120G-1-Host output characteristics at TP1a

| Parameter | Reference | Value | Units | - - |
|---|------------|------------------------------|-------|--------------|
| Signaling rate, each lane (range) | | 53.125 ± 50 ppm ^a | GBd | |
| DC common-mode output voltage (max) | 120G.5.1 | 2.8 | v | - |
| DC common-mode output voltage (min) | 120G.5.1 | -0.3 | v | - |
| Single-ended output voltage (max) | 120G.5.1 | 3.3 | v | - |
| Single-ended output voltage (min) | 120G.5.1 | -0.4 | v | - |
| AC common-mode RMS output voltage (max) | 120G.5.1 | 17.5 | mV | - |
| Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled | 120G.5.1 | 35 870 | mV | - |
| Eye height, differential (min) | 120G.3.1.5 | 10 | mV | Use CTLE/DFE |
| Vertical eye closure (max) | 120G.3.1.5 | 12 | dB | USE CILE/DFE |
| Common-mode to differential return loss (min) | 120G.3.1.1 | Equation (120G-1) | dB | |
| Effective return loss, ERL (min) | 120G.3.1.2 | 7.3 | dB | - |
| Differential termination mismatch (max) | 120G.3.1.3 | 10 | % | |
| Transition time (min, 20% to 80%) | 120G.3.1.4 | 10 | ps | [|

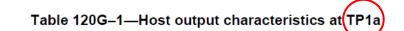


P802.3ck Electrical/Jitter Specs

100G C2M CHIP TO MODULE PHY REQUIREMENTS



Draft Amendment to IEEE Std 802.3-202x IEEE P802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force IEEE Draft P802.3ck/D2.2 1st September 2021



| Reference | Value | Units |
|------------|---|---|
| | $53.125\pm50~\mathrm{ppm}^{\mathrm{a}}$ | GBd |
| | | 1 |
| 120G.3.1.5 | 10 | mV |
| 120G.3.1.5 | 12 | dB |
| | 120G.3.1.5 | 53.125 ± 50 ppm ^a 120G.3.1.5 |

| Table 120G–3—Module output characteristics at TF | ٩4 |
|--|----|
|--|----|

| Parameter | Reference | Value | Units |
|-------------------------------------|------------|---------------------|-------|
| Signaling rate, each lane (nominal) | | 53.125 ^a | GBd |
| | | | |
| Eye height (min) | 120G.3.2.2 | 15 | mV |
| Vertical eye closure, VEC (max) | 120G.3.2.2 | 12 | dB |

TP1a is performed with TX FIR + Rx CTLE + Rx DFE for EH and VEC and requires 40GHz 4'th order Butterworth instrument response.

TP4 "far end" and "near end" are both evaluated with different tuning for reference equalization.

P802.3ck Electrical/Jitter Specs

100GBASE-CR (CABLED) INTERCONNECT PHY REQUIREMENTS

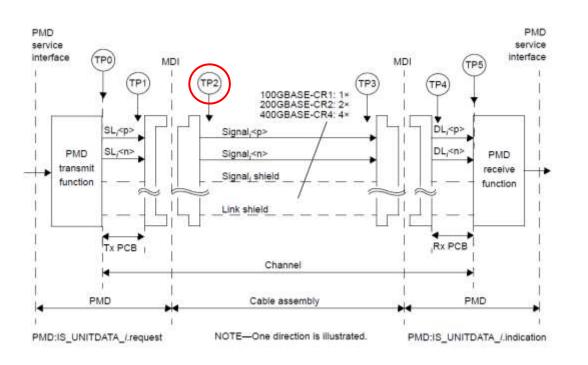


Figure 162-2-100GBASE-CR1, 200GBASE-CR2 or 400GBASE-CR4 link

TP2 is performed with TX FIR only and a 40GHz 4'th order Bessel Thomson instrument response.

TP4 is a "far end" measurement has no electrical specs associated with it.

Table 162–10—Summary of transmitter specifications at TP2

| Parameter | Subclause reference | Value | Units |
|---|-------------------------------------|---------------------------------|-------------|
| Signaling rate, each lane (range) | | $53.125 \pm 50 \text{ ppm}^{a}$ | GBd |
| Signal-to-noise-and-distortion ratio, SNDR (min) | 162,9.3.3 | 31.5 | dB |
| Output jitter (max) ^J _{RMS} J3u Even-odd jitter, pk-pk | 162.9.3.4 162.9.3.4 162.9.3.4 | 0.023 0.115 0.025 | и и и |

The recommended maximum differential-mode to differential-mode insertion loss from TP0 to TP2 or from TP3 to TP5 is 10.975 dB at 26.56 GHz. If driven by a PG, then a nominal 2dB loss should be added.

Large levels of DDG present after traversal through these loss elements and need to be compensated to within allowable limits in the TX-FFE.

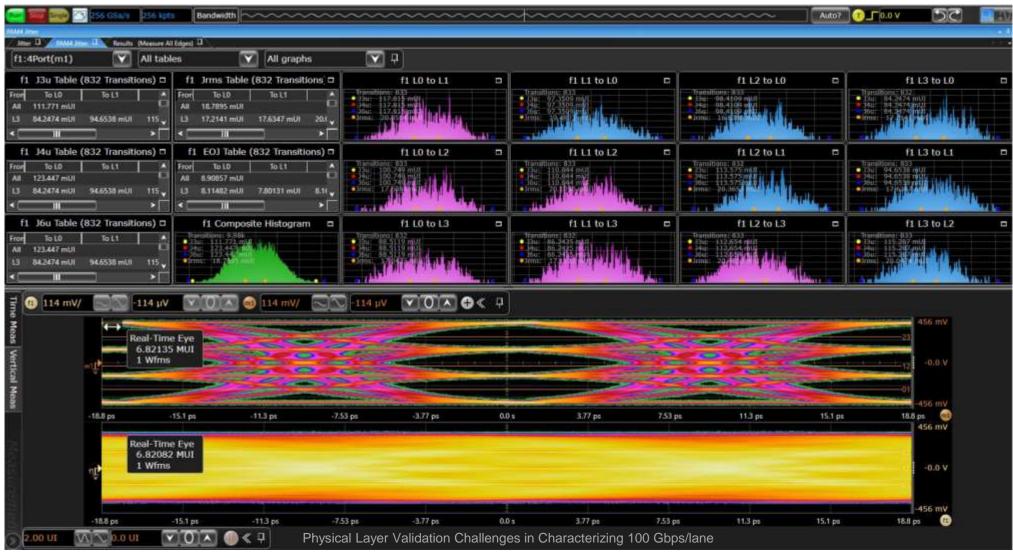


12E Operations Function on closed eye's

KEYSIGH1

TECHNOLOGIES

TYPICALLY, 10KUI'S ARE REQUIRED FOR CONFORMAL TESTS



Keysight High-Speed Digital Test Forum 是德科技高速數位量測論壇

Summary: Real-Time and Sampling Scopes

THE CORRECT INSTRUMENT FOR THE JOB DEPENDS ON REQUIREMENTS:

Real-Time Scopes (UXR)

- Early support for >112GBaud current and future modulation formats
 - High precision DSP based Clock Recovery
 - Wide Band Phase Noise analysis
 - Advanced equalization and analysis for arbitrary, burst, FEC encoded or SSC modulated patterns
 - Error Detection capabilities
- Native instrument-based error detection and BER/SER counting.
- Simple license key based bandwidth upgradeability to 113GHz

Sampling Scopes (DCA)

- Highest Signal Fidelity
 - Widest bandwidth (> 120 GHz)
 - Lowest combination of <u>noise</u> and jitter
 - Highest A/D resolution (16 bits)
- Modular platform
 - Electrical modules
 - Optical modules
 - TDR modules





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UXR and DCA DataCom Solutions

Keysight is continually engaged with emerging standards technology and offers early Beta user programs and comprehensive turn-key finished solutions to our T&M partners.

Real-time Oscilloscope (UXR) DataCom Solutions:

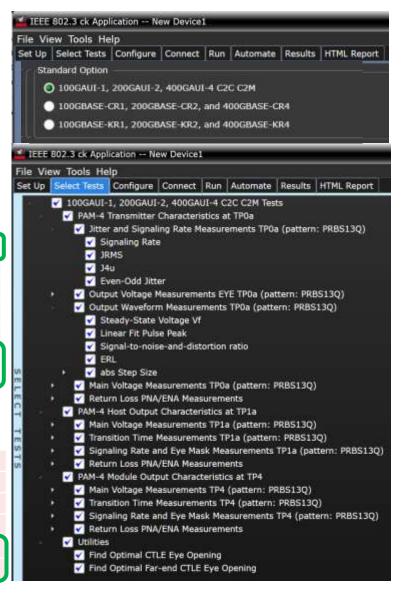
UXR-Series SW Conformance Applications

| D90103BQC | Electrical 25GBASE-T, 10GBASE-T, NBASE-T and MGBASE-T |
|-----------|--|
| D9010CAUC | 100GBASE-CR4 Electrical TX Test SW for IEEE 802.3bj (25/50/100 Gb/s) |
| D9010BJBC | 100GBASE-KR4 Electrical TX Test SW for IEEE 802.3bj (25/50/100 Gb/s) |
| D9010CEIC | Electrical TX Test SW for OIF-CEI-3.1 (56Gb/s) |
| D9010EBSC | Electrical TX Test SW for IEEE 802.3bs/cd (50/100/200/400Gb/s) |
| D90103CKC | Electrical TX Test SW for IEEE P802.3ck (C2M,C2C) (October) (KR,CR) |
| D9050CEIC | Electrical TX Test SW for OIF CEI-112Gbps/5.0 (VSR/MR/LR) |

Equivalent-Time (DCA-X, DCA-M) DataCom Solutions:

DCA Software Conformance Applications

| N109228CA | Electrical TX Test SW for OIF-CEI-3.1 |
|-----------|---|
| N1091BJCA | Electrical TX Test SW for IEEE 802.3bj (100G-KR4 and 100G-CR4) |
| N1091BMCA | Electrical TX Test SW for IEEE 802.3bm (XLAUI, CAUI-4, CAUI-10, and nPPI) |
| N1091BSCB | Electrical TX Test SW for IEEE 802.3bs/cd (50/100/200/400Gb/s) |
| N1091CKCA | Electrical TX Test SW for P802.3ck (C2M,C2C) (November) (KR,CR) |
| N109212CA | Electrical TX Test SW for OIF CEI-112Gbps/5.0 (VSR/MR/LR) |





M8091CKPA Rx Automated Closed Loop Calibration

PRE-COMPLIANCE APP FOR RECEIVERS

- Covered Standards
 - IEEE 802.3ck 100GAUI-1, 200GAUI-2 & 400GAUI-4 C2C and C2M (draft 2.1)

Key Features

- Guided setup, automated stress signal calibration & pre-compliance measurement
- Remote controlled instruments for test automation to reduce user interaction

Supported HW

- M8040A High-performance BERT
- N1000A + N1060A DCA Oscilloscope
- UXR RTS support on roadmap





Reference Material

Real-time Oscilloscope Information:

- Product Page: <u>http://www.keysight.com/find/uxr</u>
- UXR-Series Data Sheet, Lit# <u>5992-3132</u>
- UXR-Series 100G SW Conformance Solutions

Equivalent-Time (DCA-X, DCA-M) Oscilloscope Information:

- N1000A DCA-X Data Sheet, Lit# <u>5992-3271</u>
- DCA Configuration Guide, Lit# <u>5992-3372</u>
- DCA 100G SW Conformance Solutions
- FlexDCA Software Technical Overview, Lit# <u>5992-3319</u>

Other References:

- M8000 Series Bit Error Ratio Testers: <u>http://www.keysight.com/find/m8000</u>
- PNA Network Analyzers: <u>http://www.keysight.com/find/pna</u>











KEYSIGHT TECHNOLOGIES